PCT/IB2004/051819

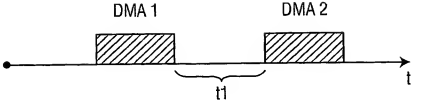

FIG. 1
PRIOR ART

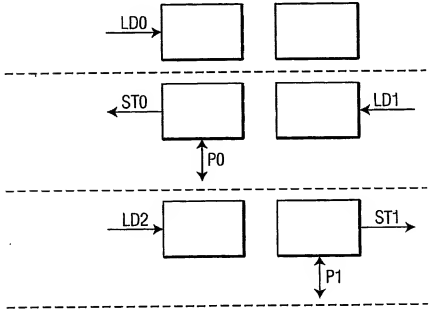

FIG. 2A
PRIOR ART

PCT/IB2004/051819

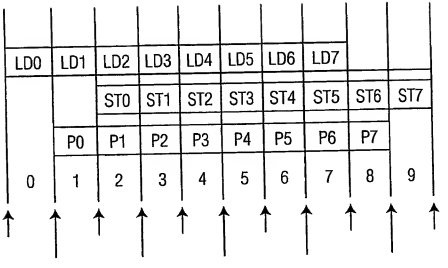

FIG. 2B
PRIOR ART

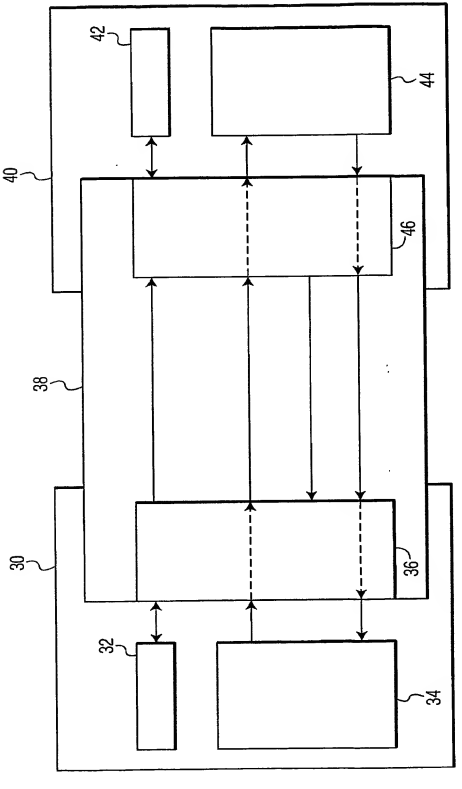

FIG. 3

PCT/IB2004/051819

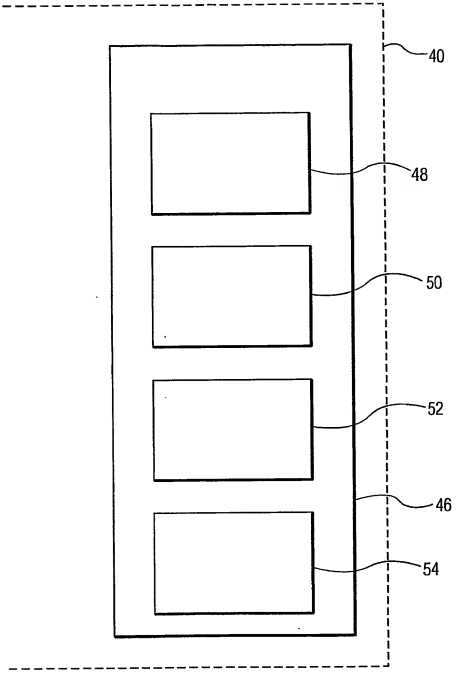

FIG. 4

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0X00		0X00		
0X04		0X04		
0X08		0X08		
0X0C		0X0C	–	
0X10		0X10	–	
0X14		0X14		
0X18		0X18		
0X1C		0X1C		
0X20		0X20		
0X24		0X24		
0X28		0X28		
0X2C		0X2C		
0X3D		0X30		
0X34		0X34		
0X38		0X38		
0X3C		0X3C		
0X40		0X40		
0X44		0X44		
0X48		0X48		
0X4C		0X4C		

FIG. 5A

PCT/IB2004/051819

0X50		0X50		
0X54		0X54		
0X58		0X58		
0X5C		0X5C		
0X6D		0X60		
0X64		0X64		
	–	0X68		
		0X6C		
	–	0X70		
		0X74		
	–	0X78		
		0X7C		
	–	0X80		
		0X84		

FIG. 5B

PCT/IB2004/051819

31:10		—	—	0x0*	
9:5	INT_ENABLE			0x0*	
4:0	INT_STATUS			0x0*	

FIG. 6A

31:10		—	—	0x0*	
9:5	INT_ENABLE			0x0*	
4:0	INT_STATUS			0x0*	

FIG. 6B

PCT/IB2004/051819

31:10		—	—	0x0*	
9:8				0x0*	
7	RX_DMA_1 _STATUS			0x0*	
6	RX_DMA_0 _STATUS			0x0*	
5	TX_DMA_1 _STATUS			0x0*	
4	TX_DMA_0 _STATUS			0x0*	
1	NEXT_TX_DMA			0x0*	

FIG. 6C

PCT/IB2004/051819

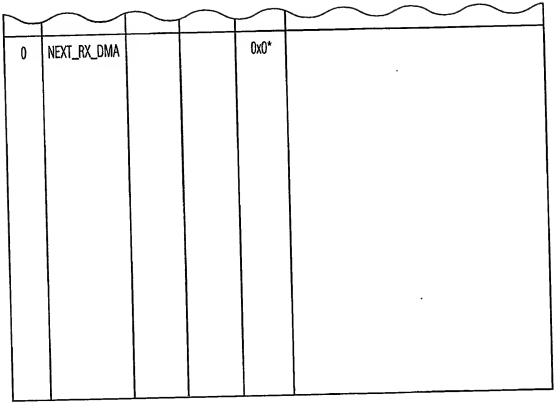

FIG. 6C1

PCT/IB2004/051819

31:10		—	—	0x0*	
9:0	MLBX_CODE			0x0*	

FIG. 6D

31:10		—	—	0x0*	
9:0	SCRCH_CODE			0x0*	

FIG. 6E

31:10		—	—	0x0*	
9:0	MLBX_CODE			0x0*	

FIG. 6F

31:10		—	—	0x0*	
9:0	SCRCH_CODE			0x0*	

FIG. 6G

PCT/IB2004/051819

31:10		—	—	0x0*	
9				0x0*	
8	DMA_msb_first			0x0*	
7	RX_DMA_1 _INT_ENABLE			0x0*	
6	RX_DMA_0 _INT_ENABLE			0x0*	
5	TX_DMA_1 _INT_ENABLE			0x0*	
4	TX_DMA_0 _INT_ENABLE			0x0*	
3	RX_DMA_1 _INT_STATUS			0x0*	
2	RX_DMA_0 _INT_STATUS			0x0*	
1	TX_DMA_1 _INT_STATUS			0x0*	
0	TX_DMA_0 _INT_STATUS			0x0*	

FIG. 6H

PCT/IB2004/051819

31:26		—		0x0*	
25:0	DMA_ADDR	—		0x0*	

FIG. 6I

31:26				0x0*	
25:0	DMA_SIZE			0x0*	

FIG. 6J

31:26		—		0x0*	
25:0	DMA_ADDR	—		0x0*	

FIG. 6K

31:16		—		0x0*	
15:0	DMA_SIZE	—		0x0*	

FIG. 6L

PCT/IB2004/051819

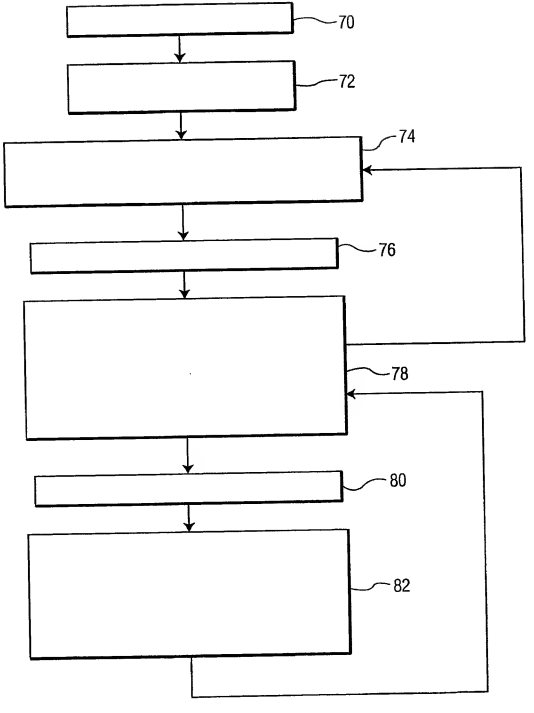

FIG. 7

PCT/IB2004/051819

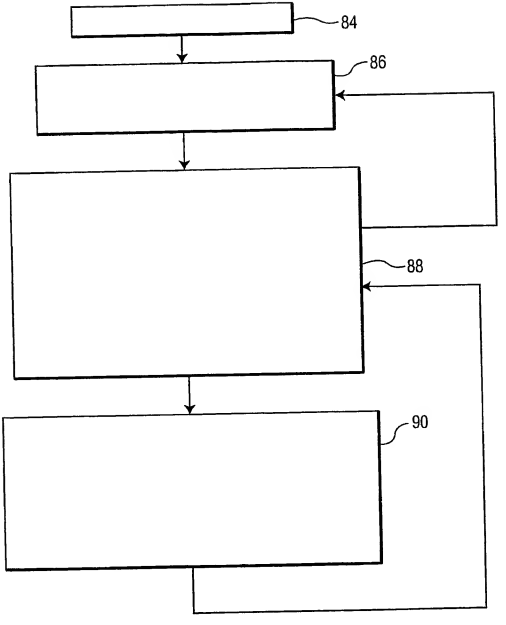

FIG. 8

PCT/IB2004/051819

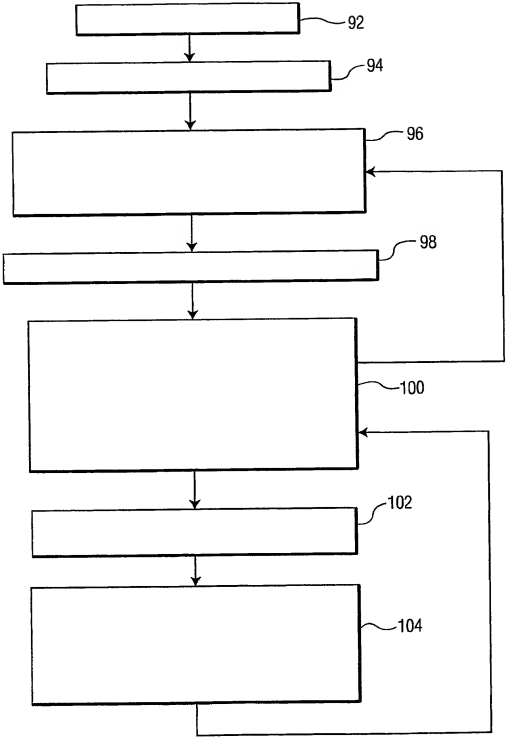

FIG. 9

PCT/IB2004/051819

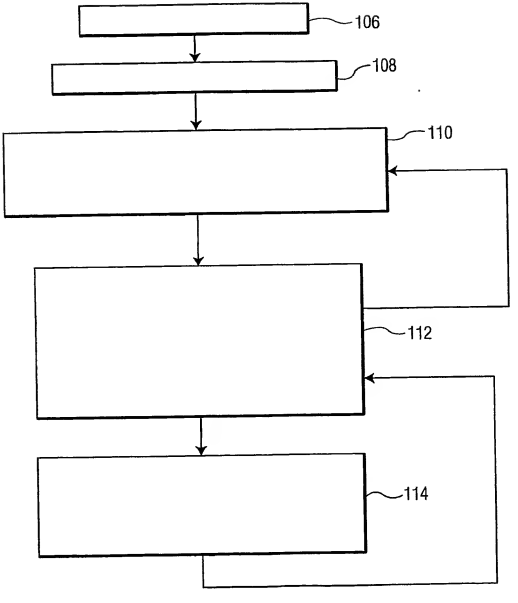

FIG. 10